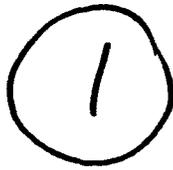


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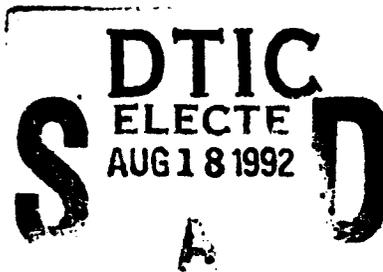
# 25 kA, 5000 V Solid State Opening Switch for Inductive Energy Stores

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JULY 1992

FINAL REPORT FOR PERIOD APRIL 1990 - APRIL 1992

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1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE July 1992	3. REPORT TYPE AND DATES COVERED Final, April 90 - April 92	
4. TITLE AND SUBTITLE 25 kA, 5000V Solid State Opening Switch for Inductive Energy Stores		5. FUNDING NUMBERS PE 63217C PR 1203 TA 03 WU 98 C: F08635-90-C-0241	
6. AUTHOR(S) Mark W. Heyse, James B. Cornette, Nolan E. Taconi, WL/MNSH Ed E. Bowles, W. G. Homeyer, John M. Rawls, General Atomics, Inc. WL Program Manager: Mark W. Heyse (WL/MNSH)			
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Wright Laboratory, Armament Directorate Analysis and Strategic Defense Division Electromagnetic Launcher Technology Branch (WL/MNSH) Eglin AFB FL 32542-5000		8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES) Same as above.		10. SPONSORING / MONITORING AGENCY REPORT NUMBER  WL-TP-92-006	
11. SUPPLEMENTARY NOTES Approved by PA for unlimited release in April 1992, published in the 6th Electromagnetic Launcher Conference proceedings. (Paper not edited by Scientific & Tech. Info. Facility.)			
12a. DISTRIBUTION / AVAILABILITY STATEMENT Approved for Public Release; distribution is unlimited.		12b. DISTRIBUTION CODE	
13. ABSTRACT (Maximum 200 words) A self-commutated solid state switch has been developed for use as an opening device for an inductive energy store. 25 kA, 5000 V operation has been obtained in a compact switch module. The switch topology is a two-stage hybrid consisting of an SCR-FET / SCR-IGBT combination. The switch is designed to charge an inductive energy store and repetitively commute the current to a dynamic load. A 25 kA switch module has been built and tested on a battery test stand at General Atomics. The theory of operation, circuit topology, and test results are given in this paper.			
14. SUBJECT TERMS  Railgun, Electromagnetic Launcher, Electromagnetic Acceleration Opening Switches, Solid State Switch			15. NUMBER OF PAGES 11
17. SECURITY CLASSIFICATION OF REPORT Unclassified			16. PRICE CODE
18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT SAR	

## PREFACE

This report documents research conducted on a solid state opening/closing switch for inductive energy store. This technical report was presented at the 6th Electromagnetic Launcher Conference in Austin, TX on 28 April to 1 May 1992.

This work was funded by the Electromagnetic Launcher Technology Branch (WL/MNSH) of the Analysis and Strategic Defense Division of the Air Force Wright Laboratory at Eglin AFB, FL under the Kinetic Energy Weapons program of the Strategic Defense Initiative. Mr Mark W. Heyse, Mr James B. Cornette and Nolan E. Taconi from WL/MNSH, and personnel from General Atomics, Inc (GA) in San Diego, Ca performed the work during the period of April 1990 to April 1992 at General Atomics in San Diego, Ca.

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# 25 kA, 5000 V SOLID STATE OPENING SWITCH FOR INDUCTIVE ENERGY STORES

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**Abstract** - A self-commutated solid state switch has been developed for use as an opening device for an inductive energy store. 25 kA, 5000 V operation has been obtained in a compact switch module. The switch topology is a two-stage hybrid consisting of an SCR-FET / SCR-IGBT combination. The switch is designed to charge an inductive energy store and repetitively commutate the current to a dynamic load. A 25 kA switch module has been built and tested on a battery test stand at General Atomics. The theory of operation, circuit topology and test results are given in this paper.

## I. INTRODUCTION

Inductive energy stores have demonstrated higher energy storage densities than capacitive energy stores. A limitation in the use of inductive energy stores has been the availability of adequately rated opening switches. A capacitive energy store needs only a closing switch to deliver energy to a load. High power closing switches are available in the form of sparkgaps, ignitrons, and SCRs. Each of these devices can momentarily conduct currents in excess of 100 kA, but once turned on they cannot interrupt current flow.

On the other hand opening switches for inductive energy stores must close and conduct current to charge the energy store and then momentarily open (interrupt the current flow) and commutate (transfer) the current to the load. Mechanical switches, GTO thyristors, and transistors are available for this opening switch duty but all have much lower power densities than closing switches.

Mechanical switches can efficiently close and conduct to charge an inductive energy store but have limited utility and lifetime in the opening phase of their duty. In contrast solid state opening switches have exceptional utility and lifetime, but suffer conduction losses and have relatively low single device current rating.

Solid state devices are generally preferred over other switch types if a performance match is available for the intended duty. The purpose of this program is to build and demonstrate a solid state opening switch which has sufficiently low conduction losses and sufficiently high power ratings to be practical in inductive energy store applications. This paper describes the design and testing of a solid state opening switch which meets these goals.

## II. THEORY OF OPERATION

Figure 1 shows a circuit schematic for the demonstration switch. It can be seen that the switch is of a hybrid design with two conduction paths and four active switching elements.

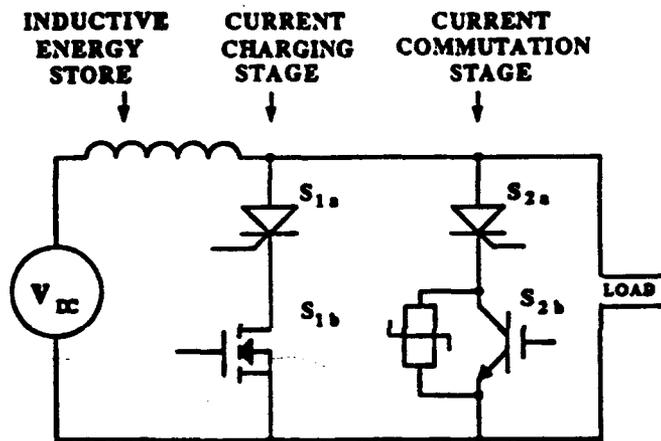


Fig. 1. Opening switch circuit schematic.

As will be explained, the different switching elements of the circuit schematic pertain to the different switching phases that an inductive energy store opening switch must support.

These phases are:

- 1) **Charge**  
Close and conduct inductor current from zero to maximum with minimum losses. Requires low conduction voltage drop.
- 2) **Commutation**  
Upon command, commutate current out of the switch and into the load by forcing a large voltage drop across the switch. Requires high commutation voltage and fast turn-off speed.
- 3) **Voltage Blocking**  
Block any voltage produced by the dynamic load and maintain zero current in the

switch. Requires high blocking voltage in the off state.

#### 4) Reclosure

Reclose and recover current from the load upon command. Requires fast turn-on speed.

These requirements have spawned the dual stage hybrid switch design shown in figure 1. The two conduction paths,  $S_1$  and  $S_2$  in Fig. 1, provide for two separate switching stages. Stage 1 (switch  $S_1$ ) provides for the low loss charging function of the switch while stage 2 (switch  $S_2$ ) provides for the forced current commutation out of the switch. Providing these two stages has allowed the switch to meet the conflicting design requirements of low conduction loss during charging and a fast, high voltage current commutation to the load.

The topology also provides for a cascode (series) connection of an SCR and a transistor in each switch stage. The charging switch stage has a 5000 V SCR in cascode with a 50 V FET transistor while the commutation switch stage has a 5000 V SCR in cascode with a 1000 V IGBT transistor. This innovative arrangement of semiconductor devices allows the transistors to accomplish the lower voltage commutation functions while the SCR accomplishes the 5000 V blocking function in a single high power device. By separating the functions of charging, commutating, and voltage blocking we have been able to provide a switch which compromises few performance attributes and has a power density approaching that of a closing switch (SCR).

Since two MOS devices (FET, IGBT) control an SCR thyristor, we call the switch a Bi-MOS Thyristor (BMT).

#### Operational Description

To see how this concept works, refer to Fig. 1. Switches  $S_{1a}$  and  $S_{1b}$  are the charging switches. Initially, the combined switch must hold off the relatively low source voltage. Both switch  $S_{1a}$  and  $S_{1b}$  are triggered into conduction to initiate the charge cycle.

When the desired current is reached and one wishes to begin the commutation process, switch  $S_{2a}$  and  $S_{2b}$  are triggered into conduction while the FET switch  $S_{1b}$  is given a gate command to increase its resistance until a 40 V drop is obtained across its terminals. This 40 V drop will commutate current out of switch  $S_1$ , and into switch  $S_2$  at a rate determined by the self inductance of the switch  $S_1$ - $S_2$  circuit. After current falls to zero in switch  $S_1$  the SCR ( $S_{1a}$ ) will begin to recover its voltage holding capabilities. The recovery time,  $t_q$ , is 275  $\mu$ s for the 5000 V SCR we have chosen. After  $\geq 275 \mu$ s of full current conduction the commutation switch, switch  $S_{1b}$ , is given a gate command to turn off. This command initiates the commutation of current from the switch to the load. The time for this commutation is determined by the inductance of switch  $S_2$

and the load circuit and the voltage produced across switch  $S_2$ .

The IGBT switch  $S_{2b}$  has a 1000 V rating and an 800 V MOV clamp across it. An IGBT turn-off time of 20  $\mu$ s is selected to provide a smooth current hand off to the MOV clamp, to maintain a reapplied  $dV/dt$  to the  $S_{1a}$  SCR of  $\leq 40$  V/ $\mu$ s, and to minimize switch  $S_{2b}$  turn-off loss. After the IGBT of  $S_{2b}$  is fully turned off, the MOVs maintain 800 V across its terminals until current is fully commutated to the load. With nominal circuit inductances this turn off process takes  $\sim 75 \mu$ s. The entire process takes  $< 1$  ms, allowing switch  $S_2$  to be pulse rated. Current in excess of five times the continuous rating of switch  $S_2$  is allowed for these short pulses.

After commutation is complete, the voltage across the switch will fall to a level dictated by the instantaneous voltage drop of the load (this voltage is generally much less than the 1000 V rating of  $S_{2b}$ ). The commutation switch SCR,  $S_{2a}$ , is allowed recovery time in the interval between current commutation and the point where the dynamic voltage produced by the load exceeds 800 V (speed voltage). After this recovery time elapses,  $\sim 100 \mu$ s for SCR  $S_{2a}$ , the entire switch is ready to support a 5000 V back voltage which is produced by the load.

A timeline which depicts the intended current and voltage waveforms for this switch is shown in Fig 2.

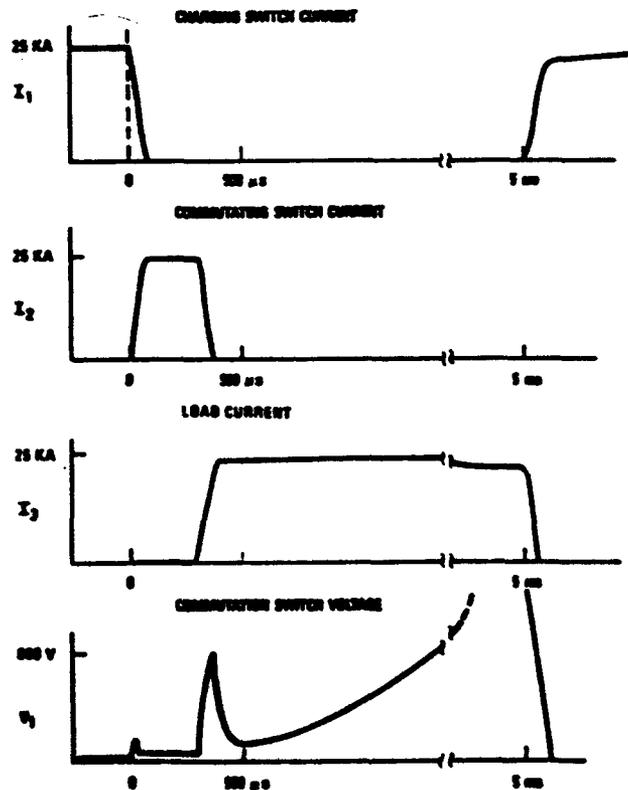


Fig. 2. Switching timeline for opening switch.

The switch can be triggered back into conduction at any time during the open phase and it is self protected to trigger back into conduction if 5000 V across the load is exceeded.

### III. CIRCUIT DESCRIPTION

A photograph of the first 25 kA, 5000 V switch module is shown in Fig. 3. The relationship of the physical arrangement of the switch module with the circuit schematic is shown in Fig. 4.

In order to achieve a 25 kA module rating several submodules were placed in parallel. A charging switch submodule consists of an ABB CS-2104, 5000 V, SCR in cascode connection with two FET modules. Each FET module consists of 96 Harris RFA100N05, 50 V FET transistors in parallel connection. The nominal 5 second current rating for each charging switch submodule is 4,166 A at a 2.35 V conduction drop. The relative distribution of the charging switch conduction drop is shown in Fig. 5a. Six conduction switch submodules are placed in parallel to achieve the 25 kA rating.



Fig. 3. Photograph of 25 kA, 5000 V opening switch.

A commutation switch submodule uses the same SCR as a conduction switch submodule and is identical in appearance. The only difference is the use of 64 Harris HGTG34N100, 1000 V IGBTs in each of the two cascode transistor modules. The nominal current rating for each

commutation switch submodule is 12,500 A at a 7.2 V drop for operation  $\leq 5$  ms for each opening cycle. The relative distribution of conduction drop is shown in Fig. 5b. Two commutation switch submodules are placed in parallel to achieve the 25 kA rating.

To complete the switch, seven Siemens B80K275 100 mm, zinc-oxide varistors are placed across the IGBT transistors in the commutation switch submodule.

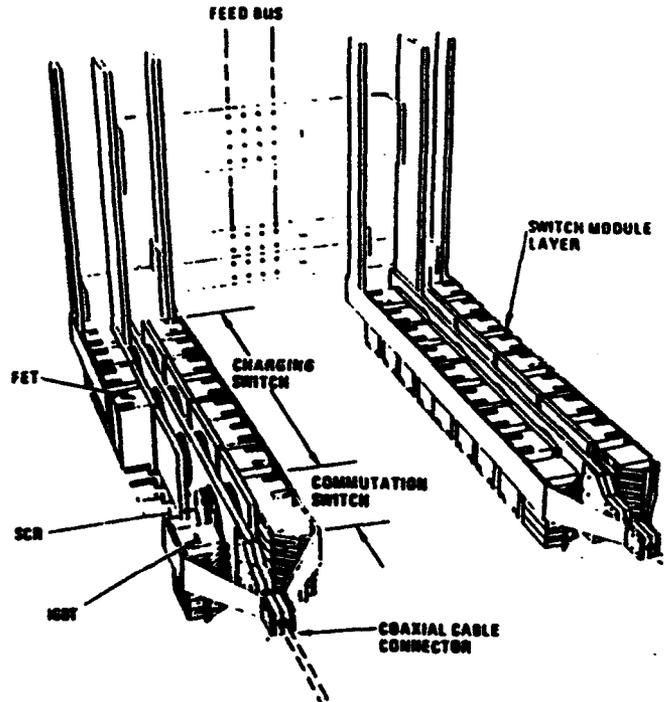


Fig. 4. Detail of physical arrangement.

#### *Parallel Operation and Current Sharing*

SCRs have nonlinear resistivity (voltage drop) and a negative temperature coefficient of resistivity. This will cause the warm SCR in a parallel array to draw more current, which drives its temperature up even more. This positive feedback effect could raise the SCR junction temperature to the point where it cannot recover and hold voltage after conduction. If an SCR in a parallel array does not recover, it will take all the current intended for the full array. SCR destruction is likely if protective action is not taken. Circuit designers typically mitigate this situation by adding series resistance and allowing for a 20-30% current mismatch. In the approach we have taken, the cascode connected FET not only forces current commutation but it forces current sharing among the SCRs. It does so by acting as a bulk resistor with a strongly positive temperature coefficient of resistivity. This SCR-FET arrangement in a submodule has a net positive temperature coefficient of resistivity at any current above 1,200 A. This factor eliminates the major concern with the parallel connection of SCRs and opens the way for arbitrarily large SCR arrays.

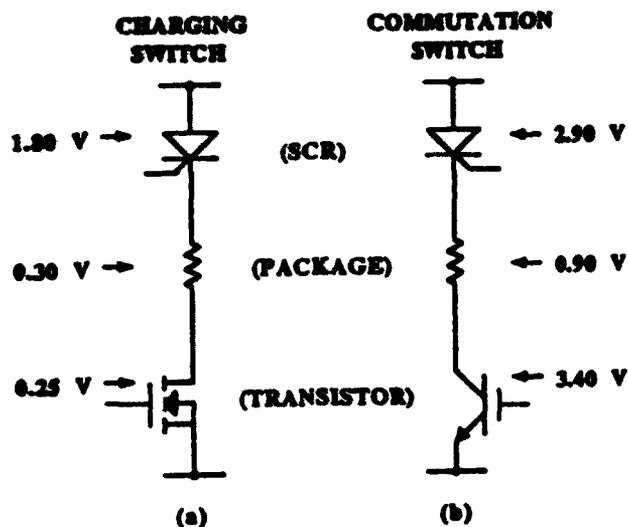


Fig. 5 (a) The relative conduction voltage drops of the charging switch components. (b) The relative conduction voltage drop of the pulse commutation switch components.

#### Thermal Management

Even with a relatively low conduction drop of 2.35 V, a 25 kA switch must reject tens of kilowatts of heat. This switch, which is intended to be used for 5 seconds at a time, lends itself to thermal inertial cooling. The copper buswork serves as a heat sink to absorb the 9.8 kW dissipated in each charging switch module. The thermal mass of the buswork is sized such that the copper temperature rises at 1°C per second with its nominal heat load. Several 5 second runs can be made before temperature limits are reached. The heat flux into the copper is such that water cooling could support continuous operation if required.

#### IV. Test Results

The 25 kA switch module shown in Fig. 3 has been successfully operated at full current at General Atomics in San Diego, California. The design margin was such that the switch survived an intentional 100% overcurrent (200% rated submodule current) for a period of 1.5 seconds. Current and voltage waveforms during a 25 kA commutation are shown in Fig. 6.



Fig. 6. Operational test results from 25 kA, full current switch operation. Top trace is switch current at 25 kA/div. Bottom trace is the load voltage at 20 V/div.

#### V. CONCLUSION

A hybrid arrangement of power semiconductor which consists of an SCR-FET / SCR-IGBT combination has been designed and built for use as an inductive energy store opening switch. Exceptional performance has been obtained with a 25 kA, 5000 V switch module using this switching topology.

#### ACKNOWLEDGMENTS

The authors would like thank Josh Kolawole of SAIC, and David Doll of General Atomics who have been of invaluable assistance with this project.

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